

USSN 10/540,268  
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843.45150X00

### **AMENDMENTS TO THE CLAIMS**

This listing of claims will replace all prior versions, and listings, of claims in the application.

#### **Listing of Claims:**

Claims 1-6 (Canceled)

7. (Currently Amended) An IC tag for transmitting first information to a reception unit while avoiding collision with transmitted information from other IC tags which transmit information to the reception unit, comprising:

a memory which memorizes the first information and second information to control the time of transmission of the first information to the reception unit; and

a memory address counter in which its count value indicates a bit address of the memory,

wherein said memory address counter and the second information have the same bit number, and wherein the IC tag sets the second information as an initial value of the memory address counter and carries out count-up of a count value of the memory address counter towards zero according to a carrier modulation signal modulated by a continuous clock signal supplied from an antenna of the reception unit, and after the count value of the memory address counter reaches zero, the first information stored in the bit address indicated by the count value is sent out to the reception unit successively to thereby avoid collision with the transmitted information from said other IC tags.

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8. (Previously Presented) The IC tag according to claim 7,  
wherein the memory memorizes third information and the IC tag sets either  
the second information or the third information as the initial value of the memory  
address counter.

9. (Previously Presented) The IC tag according to claim 8, further  
comprising a mode switching portion,  
wherein the IC tag selects the second information or the third information by  
means of the mode switching portion and sets it as an initial value of the memory  
address counter.

10. (Previously Presented) The IC tag according to claim 9,  
wherein the mode switching portion is a flip-flop and the IC tag selects the  
second information or the third information according to a value of the flip-flop and  
sets it as an initial value of the memory address counter.

Claims 11-12 (Canceled)

13. (Previously Presented) The IC tag according to claim 10,  
wherein the first information is comprised of at least an identification number  
and an error detection code for detecting an error in the identification number.

14. (Currently Amended) A reading method for reading first information  
from an IC tag having including a memory which memorizes first information and  
second information to control the time of transmission of the first information to the a  
reception unit and a memory address counter in which a count value thereof  
indicates a bit address of the memory while avoiding collision with transmitted

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information from other IC tags which transmit information to the reception unit,

comprising:

transmitting a carrier modulated signal modulated by a continuous clock signal from an antenna of the reception unit to the IC tag;

setting the second information stored in the memory as an initial value of the memory address counter; and

performing count-up of a count value of the memory address counter towards zero according to the carrier modulation signal modulated by the continuous clock signal; and

wherein said bit address counter and the second information have the same bit number, and wherein the method further comprises, after the count value of the memory address counter reaches a specified code, transmitting the first information stored in the bit address indicated with the count value successively to the reception unit to thereby avoid collision with the transmitted information from said other IC tags.

15. (Previously Presented) The reading method according to claim 14, wherein the memory memorizes third information and the second information is selected according to the mode switching signal and set up in the IC tag as the initial value of memory address counter.

Claims 16-21 (Canceled)

22. (Previously Presented) The IC tag according to claim 8, wherein the first information is comprised of at least an identification number and an error detection code for detecting an error in the identification number; and wherein the second information is a random number.

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23. (Previously Presented) The IC tag according to claim 9,  
wherein the first information is comprised of at least an identification number  
and an error detection code for detecting an error in the identification number.

24. (Previously Presented) The reading method according to claim 14,  
wherein the first information is comprised of at least an identification number  
and an error detection code for detecting an error in the identification number; and  
wherein the second information is a random number.

25. (Previously Presented) The IC tag according to claim 7,  
wherein said second information is a random number.

26. (Previously Presented) The reading method according to claim 14,  
wherein said second information is a random number.

27. (Previously Presented) The IC tag according to claim 7,  
wherein the first information identifies the IC tag.

28. (Previously Presented) The IC tag according to claim 25,  
wherein the first information identifies the IC tag.

29. (Previously Presented) The reading method according to claim 14,  
wherein the first information identifies the IC tag.

30. (Previously Presented) The reading method according to claim 26,  
wherein the first information identifies the IC tag.

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31. (Previously Presented) The IC tag according to claim 7,  
wherein the IC tag recognizes a first clock of the clock signal when the  
carrier modulation signal continues to be a high level over a specific time,  
drops to a low level, and returns to a high level after a specified time elapses.